FAD3151MXA, FAD3171MXA Gate Driver Application Note

110 V 2.5 A Single Channel Floating Gate Drivers with Desaturation Protection and Charge Pump

AND90251/D

The FAD3151MXA and FAD3171MXA are single channel floating automotive gate drivers suitable for driving high−speed power MOSFETs up to 110 V. Designed in a SOI technology, the drivers are ideal for applications that require noise immunity against severe negative transients and ground offset up to −80 V.

The FAD3151MXA/71 drivers have an integrated desaturation detection to protect the power switches during short−circuit and over−current conditions. The drivers are also equipped with a soft shutdown feature, which initiates a soft shutdown of driver outputs upon desaturation detection, thus preventing possible overvoltage across power MOSFETs during a heavy−load condition.

The FAD3151MXA/71 drivers are equipped with bidirectional fault reporting pin that generates a fault output during desat and under−voltage lockout (UVLO) condition and at the same time acts as a shutdown/disable pin for the driver. The FLT pin is in a pulled−up state for normal operation. The gate driver pulls down the FLT pin internally during desat and under−voltage lockout condition. The bidirectional nature of the fault−reporting pin allows the driver to respond to external fault commands and giving status feedback saving one pin. In addition, the FAD3171MXA has an integrated charge pump to support 100% duty cycle operation of high side MOSFETS.

In summary, the FAD3151MXA/71 are versatile drivers with features like desat detection, soft shutdown, fault reporting capability, UVLO protection, and charge pump.

Features

- Single Channel Gate Driver with +/−110 V Floating Vs Capability
- 2.5 A Output Source and Sink Current
- MOSFET Drain−Source Desaturation Detection with Soft Shutdown
- Integrated Charge Pump to Support 100% Duty Cycle Operation (FAD3171 Only)
- Under−voltage Lockout for Both Input Logic and Output Stage
- Bi−directional Fault Reporting Pin
- High Speed Driver with Short Propagation Delay
- dV_s/dt Immune to Min ±50 V/ns
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{DD} Swing on Input Pins
- SOIC−8 Package
- Pb−Free and RoHS compliant
- Automotive Qualified to AEC Q100

Typical Applications

- Gate Driver for 80 V and 100 V MOSFETs and Modules
- 48 V Belt Starter Generator
- 48 V Auxiliary Motor Control (A/C Compressor, e−Turbo, ...)
- 48 V Battery Switches
- 48 V DC−DC Converter
- PTC Heaters
- Active DC−Link Discharge Circuits

Figure 1. SOIC−8 (Case 751EB)

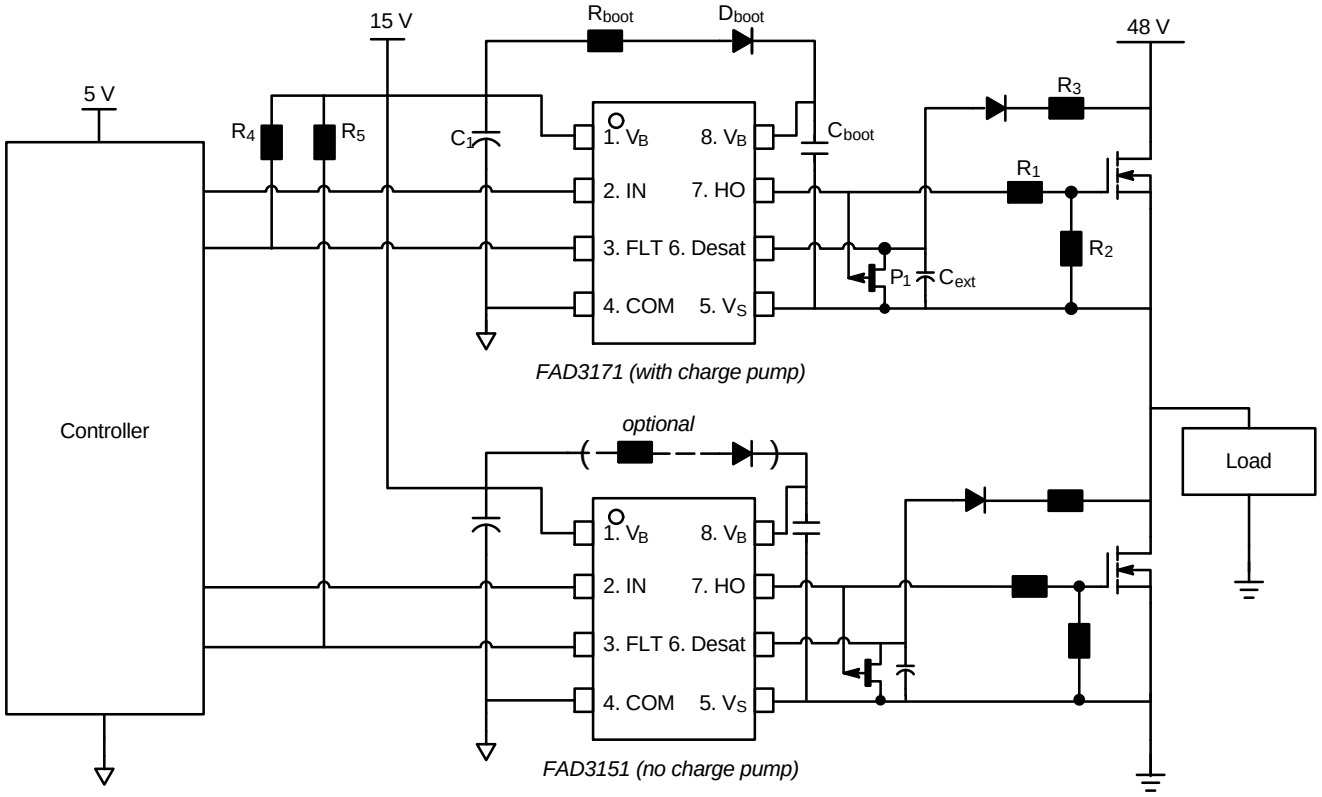

Figure 2. Application Schematic with FAD3171 as High Side and FAD3151 as Low Side Drivers

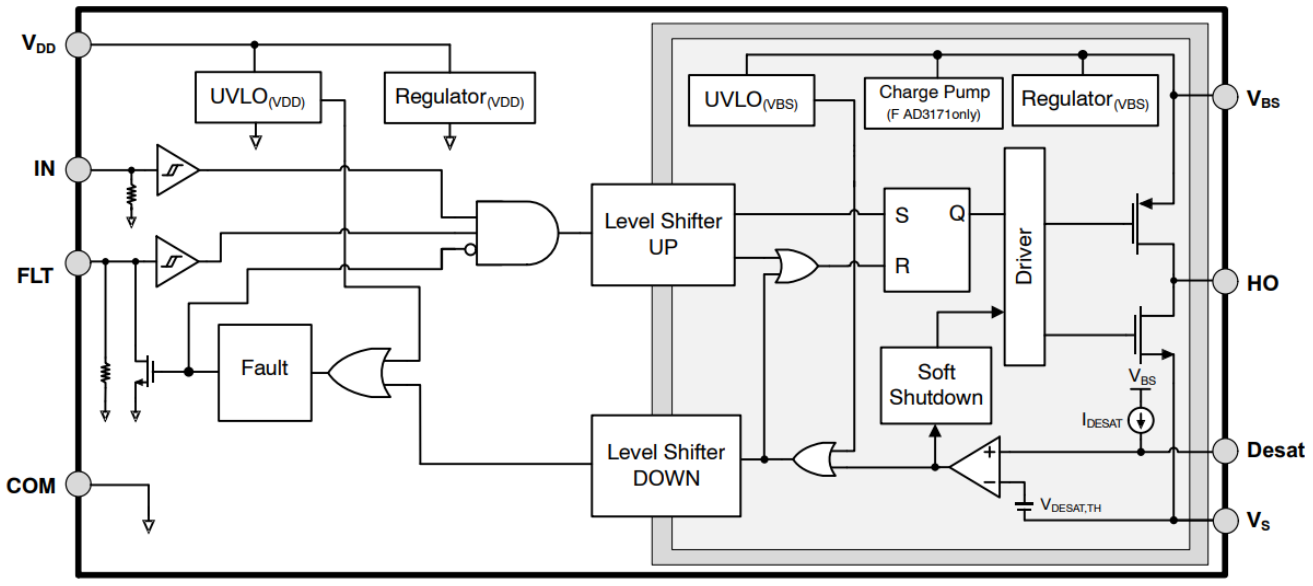

Figure 3. FAD3151 and FAD3171 (with Charge Pump) Simplified Block Diagram

PIN FUNCTION DESCRIPTION

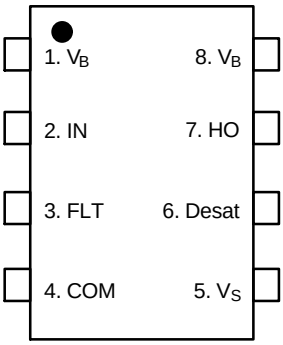

Figure 4. Pin Connection (Top View)

PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{DD}	Power supply for logic stage
2	IN	Input command
3	FLT	Bi−directional Fault pin
4	COM	Ground for logic stage
5	V_S	Floating source connection
6	Desat	Drain to Source Desaturation detection pin
7	HO	Output
8	V_B	Floating Power Supply for power stage

APPLICATION EXAMPLES

Gate Driver for 48 V DC−DC Converter Battery Switch

The simplified block diagram in Figure 5 shows how the FAD3171 can be used to drive a MOSFET as a battery main switch in a 48 V DC−DC converter.

The initial turn−on of the MOSFET is done through the bootstrap capacitance, initially charged by the 15 V supply. The integrated charge pump in the FAD3171 does not have enough source current capability to assure a direct energy efficient turn on of a larger die size MOSFET.

Once the MOSFET is turned on with 100% duty cycle, the bootstrap capacitance cannot charge any more through the 15 V supply and gets depleted by the continuous current sink into the gate to source resistance R_2 and by the internal leakage current of the gate driver.

The charge pump integrated in the FAD3171 turns on as soon as the bootstrap voltage drops below the charge pump turn on threshold, typ. 10.8 V. The charge pump operates and supplies current until the bootstrap voltage reaches the upper charge pump turn off threshold voltage (typ. 11.2 V) or, in case current consumption is too high, the bootstrap voltage drops to the driver turn off level of typ. 7.5 V.

Note that to minimize the leakage current in the gate path, the resistance R_2 should not be too low. Considering the 200 μA current sourced by the charge pump at 9 V, excluding the desat current, the resistance R_2 should be greater than 47 kΩ to maintain 9 V on the gate of the MOSFET.

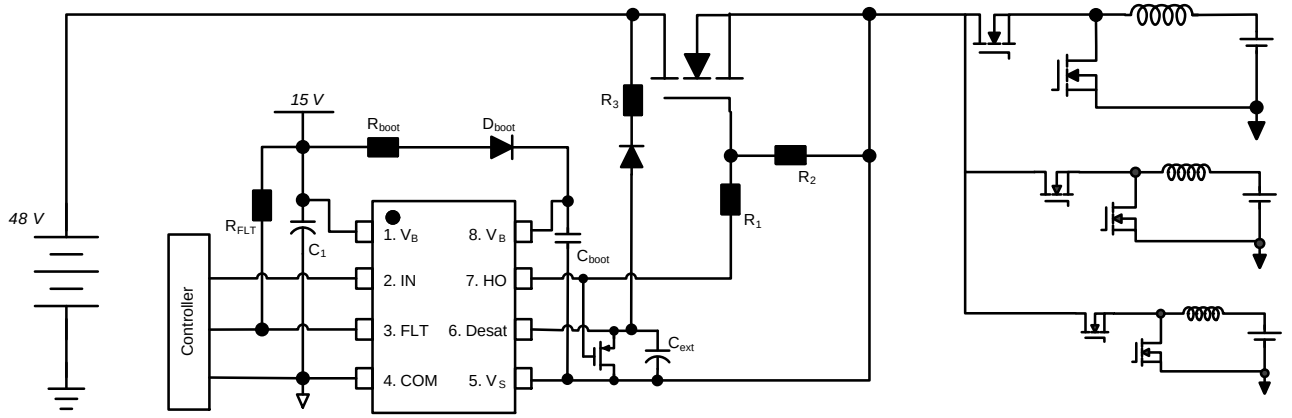

Figure 5. Gate Driver for 48 V Battery Switch

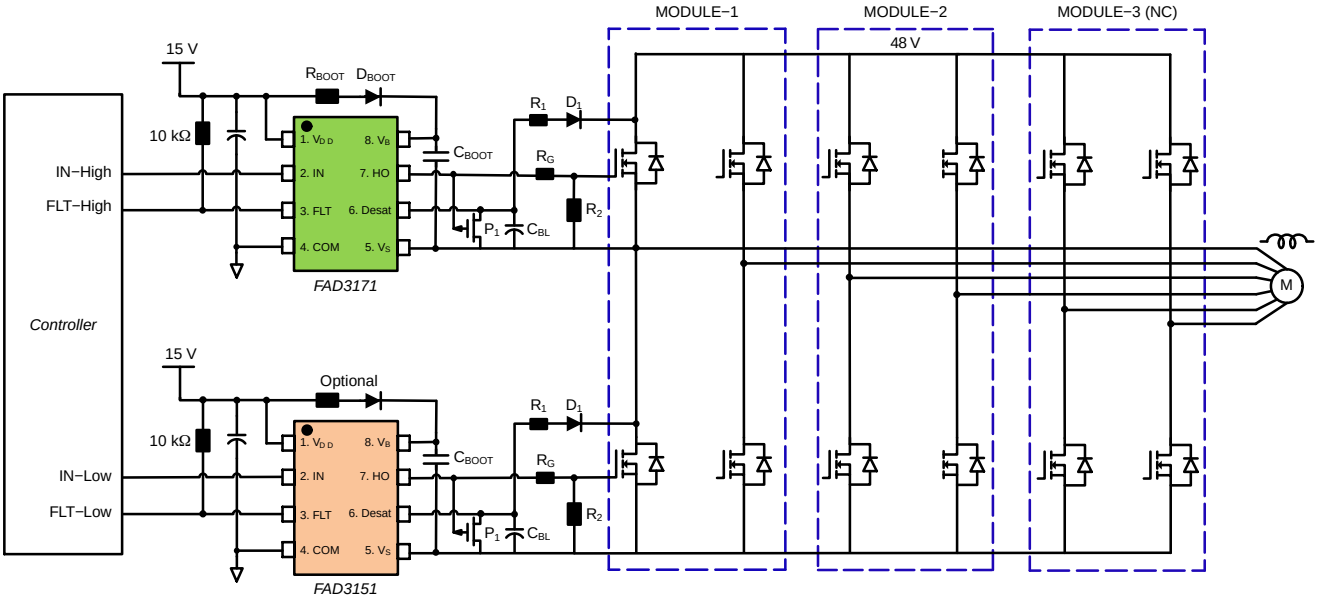

Figure 6. Gate Driver for 48 V, 3−module 6−phase Motor Control Application Circuit

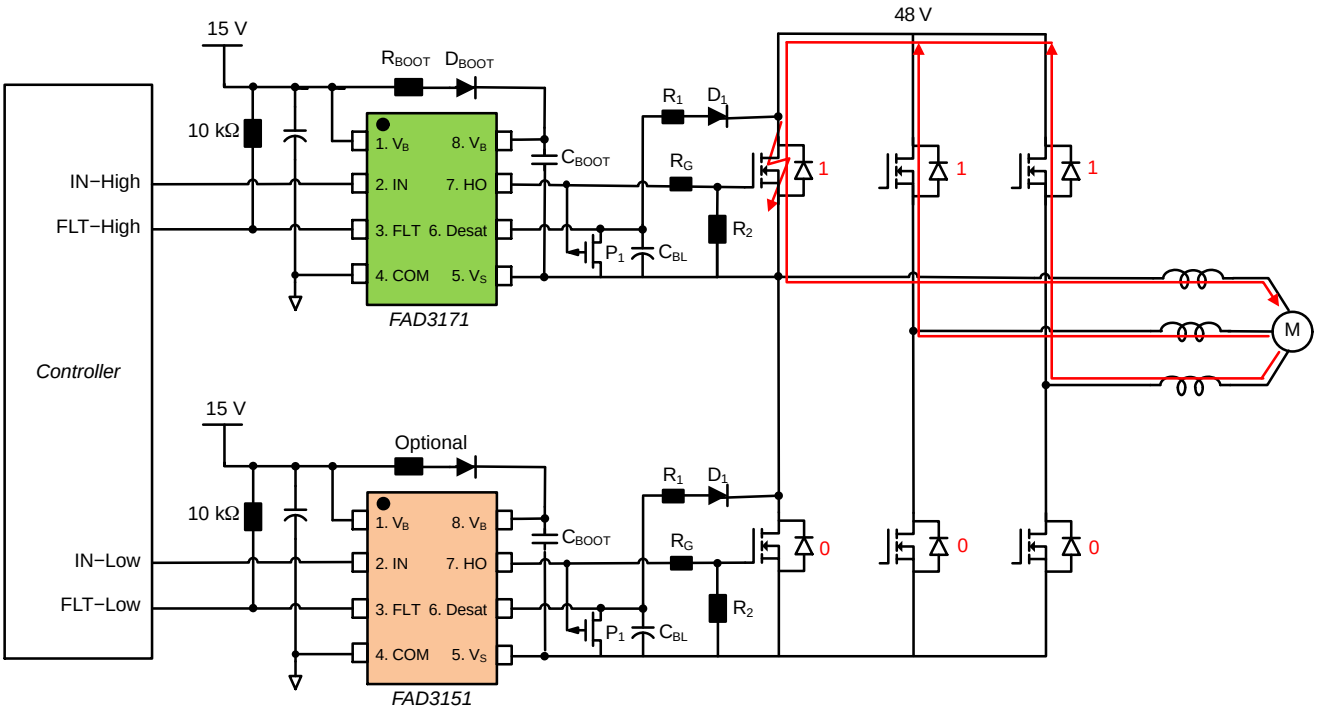

Figure 7. Gate Driver in a 3−phase Motor Control Application Circuit Operating in Active System Protection

Gate Driver for High Power Motor Control, Configured for Active System Protection

The block diagram in Figure 8 shows an example of motor control application such as a 48 V belt starter generator (BSG). The fault pins of different gate drivers are interconnected together to allow a short reaction time to turn off the affected channels upon a fault detection.

To allow current generated by the motor to discharge in the motor winding, the active turn on of the opposite channels can be programmed within the microcontroller with a simple logic as shown in Figure 8. The operation is summarized below:

- The fault pins of all High Side gate drivers are interconnected together; a fault on the High Side will:
  - Turn off all High Side gate driver outputs (controlled by the gate driver FLT_HS pins)
  - Turn on all Low Side gate driver outputs (controlled by the microcontroller control logic)
- The fault pins of all Low Side gate drivers are interconnected together; a fault on the Low Side will:
  - Turn off all Low Side gate driver outputs (controlled by the gate driver FLT_LS pins)
  - Turn on all High Side gate driver outputs (controlled by the microcontroller control logic)
- Faults on both the High Side and the Low Side gate drivers will:
  - Turn off both the High Side and Low Side gate driver outputs (controlled by the gate driver FLT_HS and FLT_LS pins)
  - To reset the fault in this case, the fault signals in the microcontroller should be bypassed with a FLT_Reset signal to allow the microcontroller to send a positive pulse on its output

By tying all fault pins together on high side or low side, an active system short−circuit protection can be achieved. During active system fault protection, either all high side or all low side switches are turned on to allow the load current to freewheel preventing overvoltage conditions and disturbances in the 48 V supply network and at the same time bringing the motor to safe state. Please refer to current flow in Figure 7.

Example of a Fault Control Logic

The Fault control logic in Figure 8 to allow active discharge is explained below:

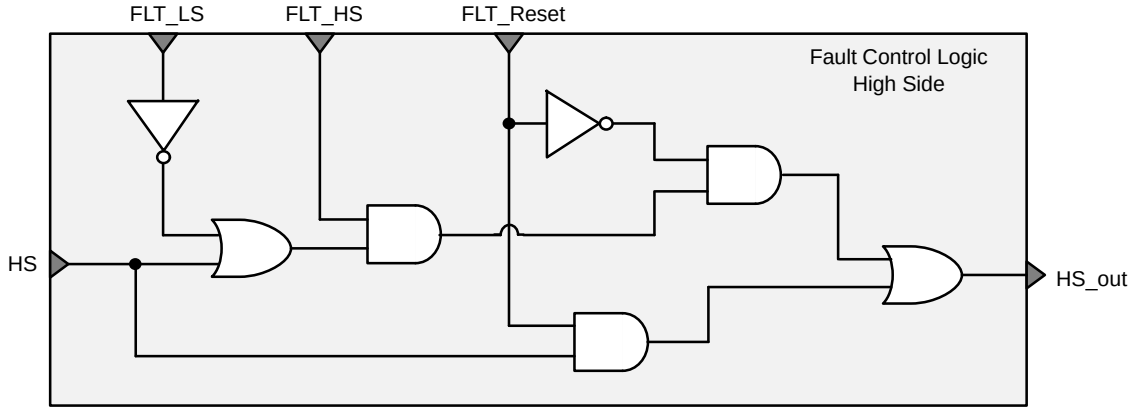

Figure 8. Example of Fault Control Logic High Side to Enable Active Discharge of Phase Current in Motor Winding

FLT_Reset is at 0 in all operation, except when a fault needs to be cleared

- If no fault on HS, FLT_HS=1
  - If no fault on the Low Side, FLT_LS=1, then HS_out=HS
  - If fault on the Low Side, FLT_LS=0, then HS_out=1 (active turn on)
- If Fault on HS, FLT_HS=0, then Phase_HS_out=0 (no active turn on for channels that have a fault)

In case both High Side and Low Side gate drivers are in fault mode, then it is not possible to apply a positive pulse on any input to clear a fault. The FLT_Reset command is used to bypass the faults and allow to apply a pulse on the input of the gate drivers to clear a fault:

- If FLT−Reset=1, then HS_out=HSFLT_LS FLT_HS

Microcontroller Interface to the Gate Driver's IN and FLT Pins

The microcontroller must have a pull up and a pull down output stage to set the input of the gate driver to high and to low. The microcontroller should, however, be able to pull up and pull down the gate driver FLT pin. It should also be able to adopt a high impedance state since the gate driver itself is able to trigger a fault by pulling down the FLT pin. This can be done with a simple pull down stage combined with a comparator to monitor the state of the FLT pin.

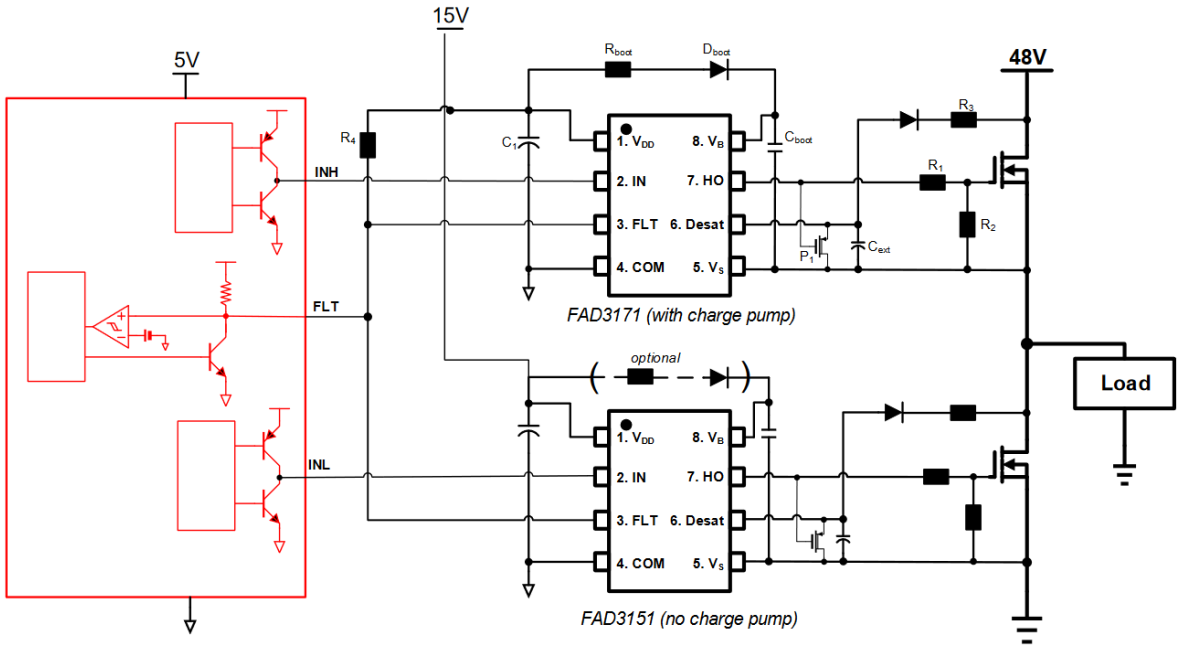

Figure 9. Microcontroller I/O Interface with the Gate Driver

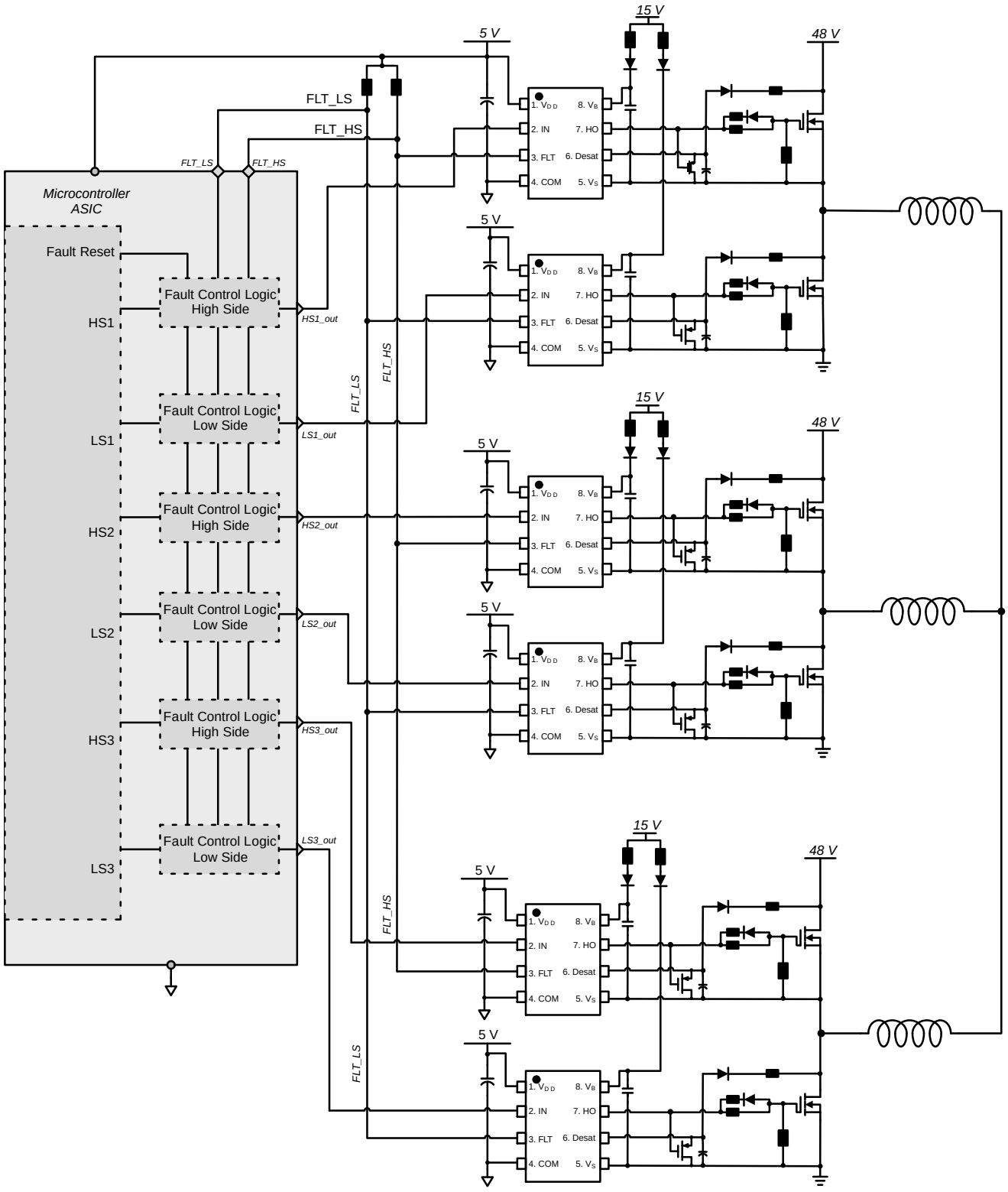

Figure 10. Block Diagram with Fault Pins Interconnected for Fault Communication

Bootstrap Drive Circuit Operation

Both the FAD3151 and the FAD3171 normally use the bootstrap technique to achieve an elevated gate drive voltage in high side operation. This bootstrap power supply technique has the advantage of being simple and low cost. However, it has some limitations. On time of duty−cycle it is limited by the time required to refresh the charge in the bootstrap capacitor.

To overcome these limitations, the FAD3171MXA driver contains an internal charge pump that enables 100% duty cycle operation of high side power switches. When the high side switch is kept on for a long duration, the bootstrap capacitor could slowly discharge and may eventually trigger the undervoltage lockout protection and turn off the driver output. Therefore, the purpose of the charge pump is to supply the V_{BS} quiescent current necessary for the high side gate driver to operate under 100% duty cycle and to compensate for additional leakage current on the gate path.

It should be ensured that the total leakage current in the gate path does not exceed the maximum output current capability of the charge pump, $I_{CP,OUT}$.

It is important to note that the charge pump is not intended to provide gate charge during switching of a power MOSFET; rather its purpose is to only keep the MOSFET turned on. For this, it should be ensured at the system level that the high side MOSFET is not operated at very high duty cycle or, if a high duty cycle operation is required, the off time should be long enough to allow the bootstrap capacitor on high side gate driver to completely recharge. In order to minimize continuous power dissipation, the charge pump turns on only when needed, and remains off at other times.

For details on the bootstrap gate−drive circuit requirements of the power MOSFET and IGBT in various switching−mode power−conversion applications and the dimensioning of the components, please refer to AN−6076: Design and Application Guide of Bootstrap Circuit for High−Voltage Gate−Drive IC. AND9674/D (onsemi.com)

Desaturation Protection Circuit

In order to protect the power stage from overload or short circuit, the FAD3151/71 features desaturation detection, which works as follows:

An internal constant current source, I_{desat}, charges an external capacitor connected to the desat pin. This allows a programmable blanking delay during every ON cycle before desat fault is processed, thus preventing false triggering. When the desat voltage goes up and reaches the desaturation threshold, V_{desat+}, the output is driven low. Further, the FLT output is activated. Please refer to data sheet Figure 19 or Figure 11 below.

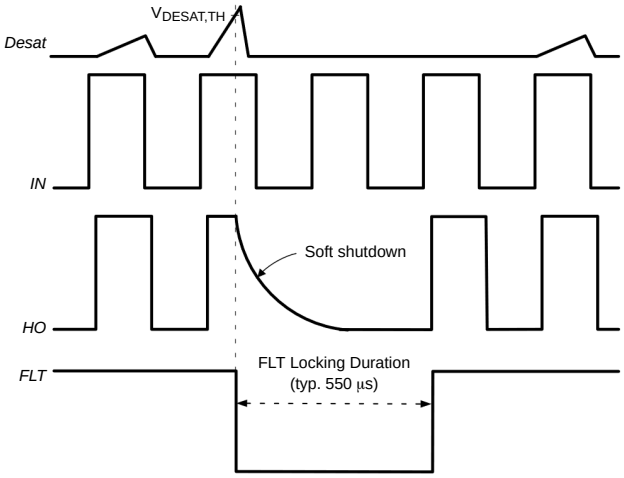

Figure 11. Desaturation Protection and Soft Shutdown

The desat terminal of the gate−driver IC monitors the drain−source voltage, V_{DS}, of the MOSFET continuously. In the event of an overcurrent or short circuit condition, the desat terminal detects a rise in V_{DS} voltage. If the desat terminal voltage exceeds V_{desat+} the gate driver IC generates a fault status and turns off the gate−drive output HO. The desat diode D_1, resistor R_1, blanking capacitor C_{ext}, and P−channel JFET P_1 are the external components required to operate the desaturation protection scheme as shown in Figure 12.

- When the gate output HO is turned off, the “normally on” discharge transistor, P_1, provides an alternate path to the desat current source, I_{desat}, and prevents it from charging the external capacitor, C_{ext}. This ensures that the desat terminal voltage is always below the desat threshold and the fault signal is not triggered during off state.
- When the gate output HO is turned on, at a voltage above ~6 V, the P−JFET, P_1, turns off. This allows the I_{desat} to charge the external capacitor, which forms a parallel circuit with D_1, R_1 and the drain to source of the MOSFET. After a period of time, t_{bl}, the desat terminal voltage, V_{desat}, stabilizes at the same level as the V_{DS} of the MOSFET plus the forward voltage of the diode D_1 and the voltage drop across the resistor R_1.

$$V_{desat} = V_{DS} + \left(V_f + R_1 \times I_{desat}\right) \quad \text{(eq. 1)}$$

- During normal operation, the V_{desat} is below the V_{desat+} and the fault pin remains disabled. During overcurrent condition, the drain to source voltage of the MOSFET rises causing the desat terminal voltage to rise as well. If the desat terminal voltage exceeds $V_{Desat+,}$ which is defined in the internal comparator stage, the gate driver generates a fault and turns off its output HO, independent of the status of the input pin.

The parameters of the desat protection circuit can be adjusted as follows:

1. The desat detection must remain disabled for a short time period called blanking time to prevent false triggering while the MOSFET first turns on. The external blanking capacitor and the desat threshold can set the blanking time. The greater the selected C_{ext}, the greater the blanking time, t_{bl}.

$$t_{bl} = C_{ext} \times V_{desat+} / I_{desat} \quad \text{(eq. 2)}$$

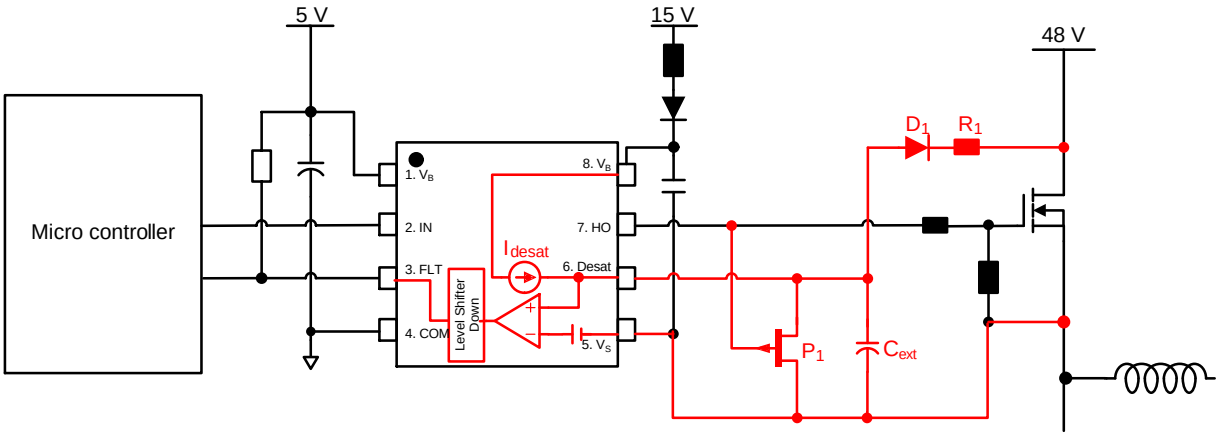

Figure 12. Desaturation Protection Circuit

2. The actual V_{DS} threshold on the MOSFET side can be modified by
   - Using a higher value of resistance R_1: With a higher R_1, the voltage at desat terminal can rise to its desat threshold at a lower V_{DS} threshold of the MOSFET. This engages desat protection at a lower V_{DS} threshold of the MOSFET. Remember:

$$V_{desat} = V_{DS} + \left(V_f + R_1 \times I_{desat}\right) \quad \text{(eq. 3)}$$

   - The selection of the desat diode is important. The desat protection works perfectly with a 200 V, 200 mA diode, which has a very low junction capacitance. When in experiments it was replaced with a generic 100 V, 1 A Schottky diode, a negative voltage spike was found to appear on the desat pin due to higher junction capacitance of this diode.

     NOTE: A low junction capacitance of the desat diode is essential for proper operation of the desat function under all operating conditions.
   - Adding multiple series diodes: Adding diodes in series can engage desat protection at a lower V_{DS} threshold of the MOSFET. However, the drawback is an additional increase in reverse recovery currents during turn−off of these diodes. The desat terminal voltage, V_{desat}, with series diodes can be expressed as:

$$V_{desat} = V_{DS} + \left(n \times V_f + R_1 \times I_{desat}\right) \quad \text{(eq. 4)}$$

     where n is the number of diodes.
   - During off state (HO low) the desat function is immune to any noise like that of capacitive coupling from adjacent switches the normally on PFET pulls the desat pin to ground. As a result, the desat pin is immune to noises when complementary FETs switches turn on and is not prone to spurious triggering.

Method for Checking the Proper Operation of the Desaturation Protection Circuit During Startup

To comply with functional safety requirements, the system might need to verify the proper operation of the desaturation protection circuit during startup. Figure 10 shows the external components necessary to perform a self−check of the desat protection circuit during startup.

- During normal operation, the self−check transistors (N_1 in high side and N_2 in low side) are turned off and the gate of P_1 is controlled by the respective gate driver output HO.
  - When HO is low, the “normally on” P_1 keeps the Cext discharged by default. As a result, the desat protection is disabled.
  - When HO is high, the gate of P_1 is pulled high through R_2, causing P_1 to turn off. As a result, Cext is free to charge and engage in desat protection.
- During self−check mode of high side gate driver, the output of the gate driver HO should be turned off and the Vs pin should be set to ground. The Vs pin can be pulled to ground by turning on the low side gate driver.
- The self−check sequence for high side desat protection circuit is as follows: (please refer to the high side components in Figure 10 and the self−check sequence in Figure 11 for details.)
  i. The microcontroller provides a high side self−check signal to turn on transistor N_1.
  ii. The PMOS P_3 turns on and pulls up the gate voltage of P_1 to V_{DD} (= 15 V) through the path V_{DD}−P_3−D_3. As a result, P_1 turns off.

iii. When P_1 turns off, the desat current flows into Cext and charges it until the voltage at the desat terminal rises to the desat threshold, Vdesat+. When Vdesat exceeds the internal Vdesat+, a fault status is triggered at the FLT pin of high side driver.

iv. The fault status is cleared when the self−check signal for high side driver is turned off.

- A malfunction of the high side desat protection circuit is detected:
  - ♦ if the high side gate driver is unable to trigger (set) a fault status on the FLT pin during self−check, or
  - ♦ if the gate driver is unable to clear this fault status at the end of self−check.
- During self−check mode of low side gate driver, the output of the high side gate driver should be turned off. The self−check sequence for low side desat protection circuit is as follows: (Please refer to the low side components in Figure 13 and the self−check sequence in Figure 14 for details.)

i. The microcontroller provides a low side self−check signal to turn on transistor N_2. At the same time, the output of the low side gate driver is turned on. As a result, P_1 turns off.

ii. When P_1 turns off, both the I_{CE} of N_2 and Idesat can charge Cext. In comparison to Idesat, the I_{CE} of N_2 could be significantly higher. Therefore, Cext is rapidly charged. When Vdesat is higher than Vdesat+, a fault status is triggered at the FLT pin of low side driver.

iii. The fault status is cleared when the self−check signal and the input signal for low side driver are turned off.

- A malfunction of the low side desat protection circuit is detected:
  - ♦ if the low side gate driver is unable to trigger (set) a fault status on the FLT pin during self−check, or
  - ♦ if the low side gate driver is unable to clear this fault status at the end of self−check.

NOTE: The desat self−check circuit shown for high side can also be adopted for low side. The low side desat self−check circuit shown in Figure 13 has fewer components than the self− check circuit on high side.

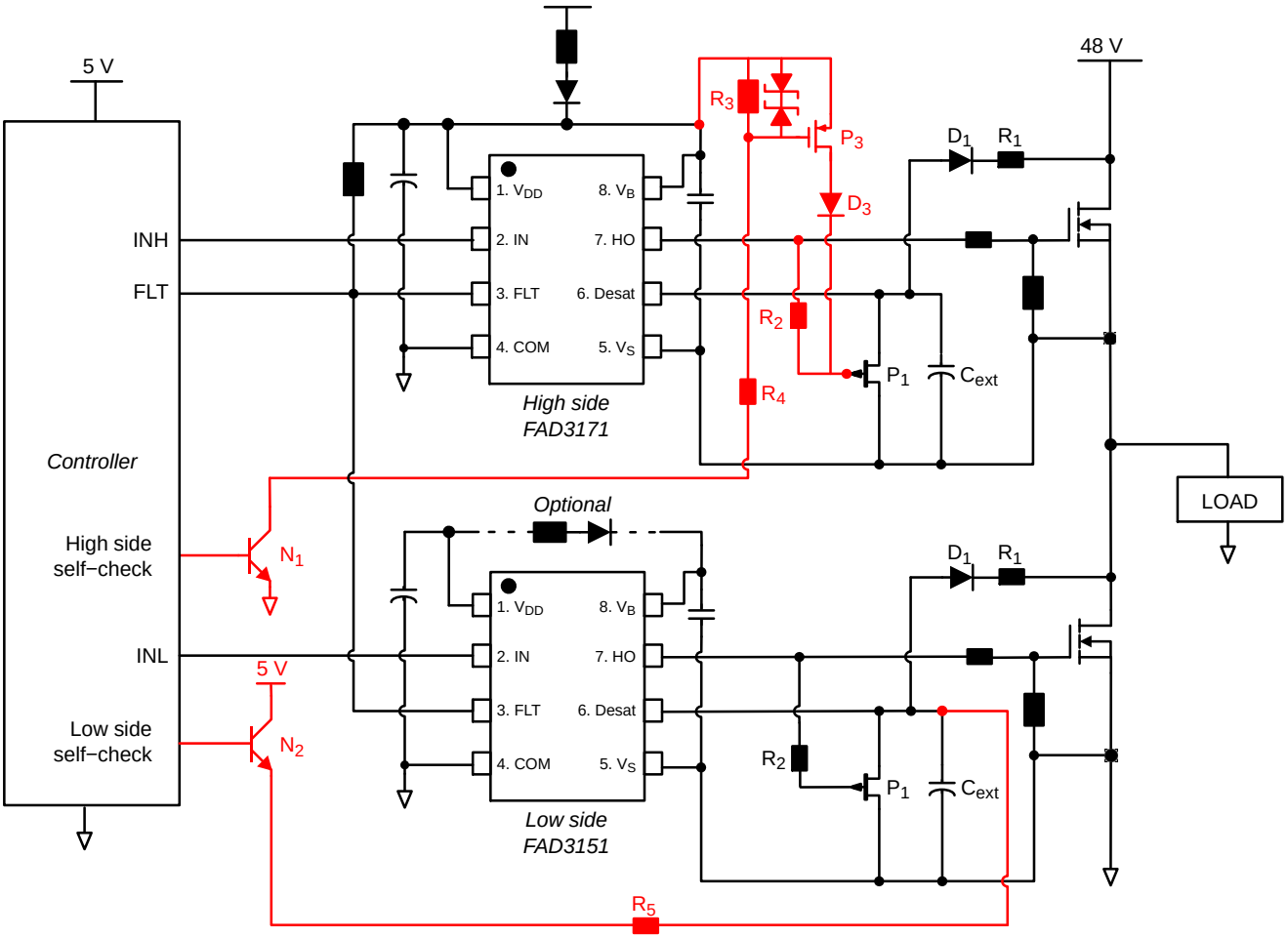

Figure 13. Circuit to Perform Self−check of the Desaturation Protection During Startup

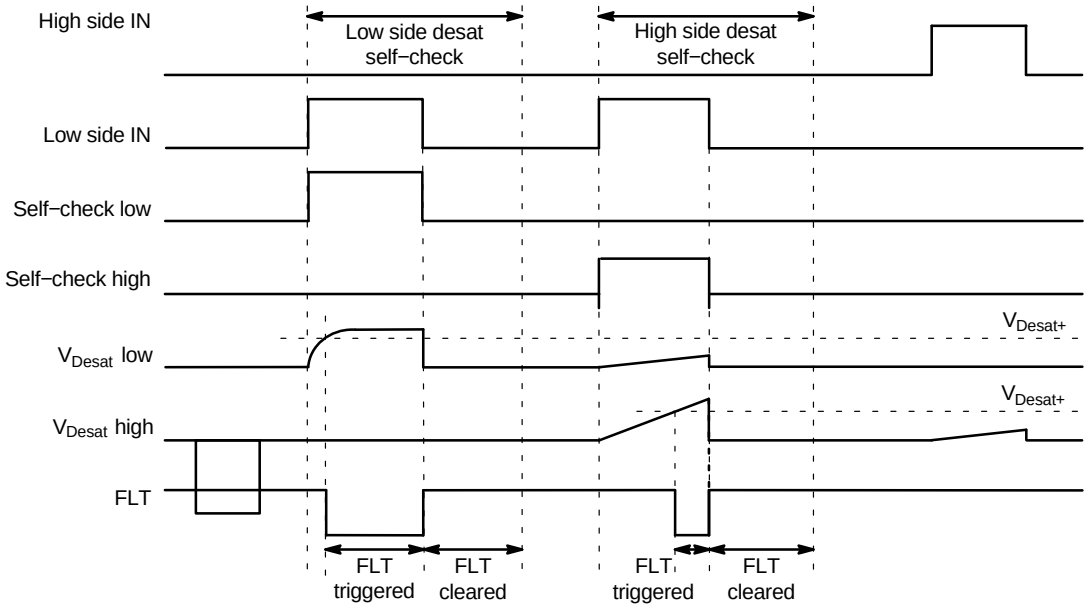

Figure 14. Self−check Sequence for High Side and Low Side Gate Driver

Considerations for Safety Critical Applications

For systems requiring functional safety, it is necessary to identify systematic failure modes that could compromise the safety of the system. The desat protection and its self−check circuit as explained in the previous chapter should be able to detect and protect against single−point failures of safety critical components. **onsemi** can support the integration into customer's safety applications with a set of safety documents including FMEDA on request.

Table 1. FAILURE MODE ANALYSIS OF THE DESAT PROTECTION CIRCUIT

Component	Failure Mode	Effect and Diagnosis of Failure	Behavior
R_1	Open	Triggers a systematic desat fault condition when HO is turned on.	Safe
	Short	Engages desat protection at a higher V_{DS} threshold of the MOSFET.	• Risk • Despite the failure, the system can operate without issue. • Mitigation: Adding two resistances in series could be an option to ensure that a single point failure does not result in a safety concern.
D_1	Open	Triggers a systematic desat fault condition when HO is turned on.	Safe
	Short	Exposes the desat pin to high voltage and could damage the gate driver.	• Risk • Mitigation: Adding two diodes in series could be an option to ensure that a single point failure does not result in a safety concern.
C_{ext}	Open	Eliminates the blanking time and causes an inadvertent triggering of desat fault during turn on of MOSFET.	Safe
	Short	• Does not allow the desat pin to reach desat threshold. • Triggers a desat fault during self−check at start up.	Safe
P_1	Open	C_{ext} is unable to discharge; triggers a systematic desat fault condition.	Safe
	Short	Does not allow the desat pin to reach its desat threshold during self−check; this can be detected during self−check as a fault status is triggered on the FLT pin.	Safe

Table 2. FAILURE MODE ANALYSIS OF THE DESAT SELF−CHECK CIRCUIT FROM FIGURE 13

Component	Failure Mode	Effect and Diagnosis of Failure	Behavior
D_3	Open	• Does not allow P_1 to turn off during self− check; this can be detected during self− check as a fault status is triggered on the FLT pin.	Safe
	Short	No issues	Safe
P_3	Open	Does not allow P_1 to turn off during self− check; this can be detected as a fault status is triggered on the FLT pin.	Safe
	Short	• Pulls up the gate of P_1 consistently. • Causes an inadvertent triggering of the desat fault.	Safe
R_2	Open	• This can be detected during self−check. • The FLT pin is able to trigger a fault status but is unable to clear it.	Safe
	Short	• Pulls down the gate of P_1 to ground and does not allow P_1 to turn off during self−check; this can be detected as a fault status is triggered on the FLT pin. • Does not affect desat protection during normal operation.	Safe
R_3	Open	Does not allow P_1 to turn off during self−check; this can be detected (FLT pin is able to set the fault status but unable to clear it).	Safe
	Short	Does not allow P_3 to turn on (and P_1 to turn off); this can be detected as a fault status is triggered on the FLT pin.	Safe
R_4	Open	Does not allow P_3 to turn on (and P_1 to turn off) during self−check; this can be detected as a fault status is triggered on the FLT pin.	Safe
	Short	No issues	Safe
N_1	Open	Does not allow P_3 to turn on (and P_1 to turn off) during self−check; this can be detected as a fault status is triggered on the FLT pin.	Safe
	Short	Does not allow P_3 to turn off (and P_1 to turn off) during self−check; this can be detected as the FLT pin is unable to clear the fault status.	Safe
N_2	Open	A fault status is not triggered during self−check; this can be detected.	Safe
	Short	the Cext is never discharged. Causes an inadvertent triggering of the desat fault.	Safe
R_5	Open	A fault status is not triggered during self−check; this can be detected.	Safe
	Short	No issues.	Safe

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